02-13-04 Image AF/$

Attorney's Docket No. 67,200-477 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In application of: Chen et al
Serial No.: 09/ 941,537
Filed: Aug. 29, 2001
For: Method for Reducing Light Reflectance in a Photolithographic Dual Damascene Trench Patterning Process

Group Art Unit: 1756
Examiner: J.S. Ruggles

Commissioner for Patents
Alexandria, VA 22313

TRANSMITTAL OF APPEAL BRIEF (PATENT APPLICATION-37 CFR 192)

1. Transmitted herewith, in triplicate, is the APPEAL BRIEF in this application, with respect to the Notice of Appeal filed on Dec. 11, 2003 .

NOTE: "The Appellant shall, within 2 months from the date of the notice of appeal under §1.191(a) or within the time allowed for response to the action appealed from, if such time is later, file a brief in "triplicate", 37 C.F.R. 1.192(a) [emphasis added].

2. STATUS OF APPLICANT
This application is on behalf of:
X other than a small entity.
___ a small entity.

A verified statement:
___ is attached.
___ was already filed.

3. FEE FOR FILING APPEAL BRIEF
Pursuant to 37 CFR 1.17(f), the fee for filing the Appeal Brief is:

___	small entity	$165.00
X	other than a small entity	$330.00

Appeal Brief fee due: $ 330.00

Certificate of Mailing/Transmission (37 CFR 1.8(a))

I hereby certify that this correspondence is, on the date shown below, being:

Mailing
X deposited with the U.S. Postal Service
with sufficient postage as Express Mail
Label No. EV 405 451 688 US
in an envelope addressed to Commissioner
for Patents, Alexandria, VA 22313

Kathy Dixon

Dated: Feb. 11, 2004

4. EXTENSION OF TERM

NOTE: The time periods set forth in 37 CFR 1.192(a) are subject to the provision of ☐1.136 for patent applications. 37 CFR 1.191(d). See also Notice of November 5, 1985 (1060 O.G. 27).

The proceedings herein are for a patent application and the provisions of 37 CFR 1.136 apply:

(complete (a) or (b), as applicable)

(a) ☐ Applicant petitions for an extension of time under 37 CFR 1.136 (fees: 37 CFR 1.17(a)-(d) for the total number of months checked below:

	Extension (months)	Fee for other than small entity	Fee for small entity
☐	one month	$ 110.00	$ 55.00
☐	two months	$ 420.00	$210.00
☐	three months	$ 950.00	$475.00
☐	four months	$1,480.00	$740.00

Fee: $_____

If an additional extension of time is required, please consider this a petition therefor.

(check and complete the next item, if applicable)

☐ An extension for _____ months has already been secured, and the fee paid therefor of $_____ is deducted from the total fee due for the total months of extension now requested.

Extension fee due with this request: $_____

or

(b) ☐ Applicant believes that no extension of term is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition and fee for extension of time.

5. TOTAL FEE DUE

The total fee due is:

Appeal Brief Fee: $ 330.00
Extension fee (if any) $_____

TOTAL FEE DUE: $ 330.00

6. FEE PAYMENT

X Attached is a Credit Card Payment Form for the sum of $ 330.00

A duplicate copy of this transmittal is attached.

7. FEE DEFICIENCY

NOTE: If there is a fee deficiency and there is no authorization to charge an account, additional fees are necessary to cover the additional time consumed in making up the original deficiency. If the maximum six-month period has expired before the deficiency is noted and corrected, the application is held abandoned. In those instances where authorization to charge is included, processing delays are encountered in returning the papers to the PTO Finance Branch in order to apply these charges prior to action on the cases. Authorization to charge the deposit account for any fee deficiency should be checked. See the Notice of April 7, 1986, 1065 O.G. 31-33.

__X__ If any additional extension and/or fee is required, this is a request therefor to charge Visa Credit Card No. 4756 8461 9568 0263

And/Or

__X__ If any additional fee for claims is required, please charge Visa Credit Card No. 4756 8461 9568 0263

Signature of Attorney

Registration No. 31,311

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Applicant: Chen et al. Group Art Unit: 1756

Serial No.: 09/941,537 Examiner: J. S. Ruggles

Filed: 08/29/2001

For: METHOD FOR REDUCING LIGHT REFLECTANCE IN A PHOTOLITHOGRAPHIC DUAL DAMASCENE TRENCH PATTERNING PROCESS

Attorney Docket No.: 67,200-477

EXPRESS MAIL CERTIFICATE

Express Mail label Number EV 405 451 688 US
Date of Deposit Feb-11/04

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Kathy Dixon

APPEAL BRIEF

Mail Stop: Appeal
Commissioner for Patents
Alexandria, VA 22313-1450

Sir:

Appellant appeals in the captioned application from the Examiner's final rejection, dated 11/28/2003, of claims 1-3, 7-8, 10-11, 13-15, and 17-26, under 35 USC § 103.

It is urged that Examiners final rejection be reversed and that all the claims currently pending be allowed.

(1) REAL PARTY IN INTEREST

The real party in interest in the present appeal is the recorded Assignee of Taiwan Semiconductor Manufacturing Company, Ltd.

(2) RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences that are known to the Appellant, the Appellant's legal representative, or the assignee.

(3) STATUS OF CLAIMS

Claims 1-3, 7-8, 10-11, 13-15, and 17-26 are pending in the application.

Claims 1-3, 7-8, 10-11, 13-15, and 17-26 stand rejected.

(4) STATUS OF AMENDMENTS

A Request for Reconsideration was filed on or about 09/11/2003.

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suggested by Examiner and canceling claim 25 and 26 to overcome Examiners objections. The first supplemental includes proposed amendments to claims 11 and 18 to overcome Examiners rejection under 35 USC 112, second paragraph relating to grammatical errors to remove these issues from Appeal. To Appellants knowledge, the first supplemental amendment is pending, however the claims are presented in the Claims Appendix assuming the amendments have been entered since they relate to grammatical and typographical errors and remove issues on appeal.

A second supplemental amendment was filed on or about 2/11/2004 further amending the Specification to overcome Examiners rejection under 35 USC 112, second paragraph with respect to claim 15. To Appellants knowledge, the second supplemental amendment is pending.

(5) SUMMARY OF THE INVENTION

The invention discloses a method for reducing light reflectance from via sidewalls in a photolithographic trench patterning dual damascene process to reduce undercutting of a photoresist layer thereby maintaining design distance between metal lines. (See Field of Invention Specification, paragraph

001; claim 1; Figures 2, items 25 and 26 and Figure 3, items 35 and 36). The method involves the steps of providing an inter-metal dielectric (IMD) layer comprising at least one via opening extending through a thickness thereof; forming an antireflectance coating (ARC) layer over the IMD layer such that the ARC layer is formed over sidewalls of the at least one via opening without filling the at least one via opening; and, depositing a photoresist layer over the IMD layer and photolithographically patterning a trench opening over the at least one via opening.

(6) **ISSUES**

1. Is the rejection of claim 15, under 35 USC second 112, second paragraph proper?

2. Is the rejection of claims 1-3, 7-8, 10-11, 13-15, and 17-24 under 35 USC § 103(a) as being unpatentable over Lin et al. (US 6,042,999) in view of Yu et al. (US 6,027,861) and further in view of Filipiak et al. (US 5,918,147) proper when such references does not teach or suggest the specifically claimed limitations in the present application?

(7) GROUPING OF CLAIMS

The claims 1, 2, 10, 11, 18, and 20 do not stand and fall together.

(8) ARGUMENTS

Issue 1

Claim 15 stands rejected under 35 USC 112, second paragraph. Examiner claims that the claim, presented in standard Markush claim format is unclear. Examiner supports this argument by asserting that APPELLANTS disclosure only supports silicon oxynitride or silicon nitride for the first etching stop layer. APPELLANTS assert that this is improper argument under 35 USC 112, second paragraph, where Examiner is attempting to assert his interpretation of the Specification including interpreted limitations into a claim that is clear on its face. APPELLANTS disagree with Examiners interpretation, and suggest Examiner if anything, should have objected rather than rejected the claim. APPELLANTS have filed a second supplemental amendment with the Appeal brief inserting the language in claim 15 into the Specification to remove this issue from appeal.

Issue 2

Claims 1-3, 7-8, 10-11, 13-15, 17-24 stand rejected under 35 USC 103(a) as being unpatentable over Lin et al., in view of Yu et al. (US Pat.No. 6,027,861) and further in view of Filipiak et al. (US Pat. No. 5,918,147).

a) Lin et al. teach a dual damascene process **by filling a via opening** with **protective material** prior to patterning an overlying trench in a dual damascene process (see Abstract). The protective material serves to protect the exposed material at the bottom of the via opening during a subsequent overlying trench etching process (see e.g., col 6, lines 10-14). Lin et al. teach first forming a via opening portion (see e.g., col 4, lines 55-67, col 5, lines 20-25). After removing the via pattern resist layer, Lin et al. teach depositing a protective material disclosed to be a BARC layer e.g., silicon oxynitride or an organic material **to fill the via opening**, (see e.g., col 5, lines 35-57, Figure 2C). Lin et al. then teach removing a portion of the protective material **from the filled via opening** to about a level of an intervening etch stop layer following patterning of the overlying trench. The protective material is first etched back followed by etching of the overlying trench or

simultaneously etched back with the trench etching (see col 5, lines 57-65 and col 5, lines 1-14).

Examiner argues "while not specifying an alternative embodiment requiring non-filling of the ARC layer in the holes or openings, it is readily apparent that adequate protection could also be obtained by using one or more ARC layers of sufficient thickness without necessarily requiring that the ARC material fill one or more via openings or holes.." . Examiner is impermissibly re-creating APPELLANTS disclosed invention by hindsight reasoning and can point to no suggestion, hint, or desirability in Lin et al. for doing what APPELLANTS have accomplished by their claimed invention.

The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." *In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).*

Examiner argues that the prior art disclosed in Lin et al. as shown in Figures 1C through 1F support Examiners argument since "these etch stop materials are also expected to inherently

function as ARC layers". Examiner provides no support for this statement of inherency. Lin et al. only disclose the use of SiN as an etch stop layer. Nevertheless, the fact that SiON is well known as having antireflectance properties is irrelevant to the issue of whether APPELLANTS claimed invention has been suggested or disclosed in Lin et al.

The prior art as disclosed in Lin et al. is referring to a totally different process of manufacturing dual damascenes. The prior art e.g., at col 2, lines 34-52) discloses depositing a **selective etch barrier layer** where SiN or SiON are disclosed to be useful materials with an appropriate etching selectivity. The etch barrier is deposited into **a trench opening** followed by etching **an opening through the etch barrier** at the bottom of the trench opening **followed by etching the via hole**. The etch barrier disclosed in the prior art by Lin et al. is not suggested or disclosed to have or require an anti-reflective property. However, even assuming arguendo, that such a suggestion was present in Lin et al., the teachings of Lin et al. do not produce APPELLANTS disclosed and claimed invention nor recognize or solve the problem that APPELLANTS have recognized and solved in their claimed invention:

"A method for reducing light reflectance from via sidewalls in a photolithographic trench patterning dual damascene process comprising the steps of:

forming an antireflectance coating (ARC) layer over the IMD layer such that the ARC layer is formed over sidewalls of the at least one via opening **without filling the at least one via opening**; and,

depositing a photoresist layer over the IMD layer and photolithographically patterning a trench opening over the at least one via opening."

Moreover, the prior art disclosed in Lin et al. that the Examiner relies on, would not work in the method of APPELLANTS since the purpose of the ARC layer is to reduce reflections in an overlying trench line patterning process **following formation of a via opening**. Indeed, Lin et al. affirmatively teach away from APPELLANTS claimed invention by requiring either a separate or simultaneous etching step to remove a portion of the protective material during etching an overlying trench (col 5, line 62 - col 6, line 14). The principal of operation of Lin et al. is completely different than the principal of operation of the method of Lin et al.

"Obviousness can only be established by combining or modifying the

teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art." *In re Fine, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988); In re Jones, 958 F.2d 347, 1 USPQ2d 1941 (Fed. Cir. 1992).*

"If the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims prima facie obvious." *In re Ratti, 270 F.2d 810, 123, USPQ 349 (CCPA 1959).*

"To establish inherency, the extrinsic evidence must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill." *In re Oelrich, 666 F.2d 578, 581-582, 212 USPQ 323, 326 (CCPA 1981).*

Lin et al., further do not teach, suggest or disclose forming a first ARC layer over the IMD layer **prior** to forming via openings followed by **forming** a second ARC layer to cover via opening sidewalls **without filling the at least one via opening** as claimed by APPELLANTS in amended claim 11. Neither do Lin et al. disclose the problem of photoresist undercutting from via sidewall reflections or disclose APPELLANTS claimed limitations in claims 10, and 18.

Lin et al. further do not teach forming a first ARC layer prior to forming the via opening and a second ARC layer to cover via opening sidewalls following formation of a via opening as claimed by APPELLANTS in independent claim 11 and 20 and independent claim 20, or including an etch stop layer over the IMD layer as claimed in claims 2, 13, and 20 (second dielectric layer). Examiner has not made out a *prima facie* case of obviousness according to Lin et al. with respect to above limitations.

b) Yu et al. teach a method for etching sub-quarter micron openings in dielectric insulating layers by using a thin layer DUV photoresist (see Abstract). In one embodiment, Yu et al. disclose forming a via opening for filling with a tungsten plug by using a Ti/TiN etching hardmask which also functions as an ARC layer for etching the via opening (col 4, lines 58-62). The via is then etched with the Ti/TiN layer hard mask providing high selectivity for etching the insulating layer (col 6, lines 19-24).

Yu et al. does not suggest disclose or suggest depositing an ARC layer to fill the via opening as taught by Lin et al., nor disclose or suggest forming an ARC layer formed over sidewalls of

a via opening without filling the via opening prior to patterning an overlying trench portion in a dual damascene process as claimed by APPELLANTS.

There is no apparent reason for combining the teachings of Yu et al. with Lin et al. However, even assuming *arguendo* proper combination of Yu et al. and Lin et al., such combination does not produce APPELLANTS claimed invention. The disclosure of Yu et al. in forming a Ti/TiN hardmask layer that also functions as an ARC layer does not help Examiner in making out a *prima facie* case of obviousness. APPELLANTS do not disclose or claim a Ti/TiN layer but rather disclose a TiN ARC layer as one element of a Markush group for forming a first or second ARC layer. Yu et al. do not discuss, disclose or suggest the desirability of depositing an ARC layer to cover the via opening sidewalls without filling the via opening prior to a trench patterning process overlying the via. The teachings of Yu et al. do not recognize or solve the problems APPELLANTS have recognized and solved by their claimed invention. Yu et al. does not help Examiner in establishing a *prima facie* case of obviousness.

c) Filipiak et al. generally discloses types of ARC layers such as silicon oxynitride and titanium nitride in the background of

the invention (see col 1, lines 10-20) as well as teaching the use of multiple ARC layers including forming inorganic ARC layers, e.g., silicon oxynitride with a continuously graded composition or including a plurality of discrete portions that make up the antireflective layer (see col 2, lines 17-27, col 3, lines 21-30). There is no apparent motivation for combining Filipiak et al. with either Yu et al. or Lin et al. For example, Filipiak et al. disclose the use ARC layers **prior to** etching via openings, and further, do not disclose a dual damascene process.

Nevertheless, assuming *arguendo*, a proper motivation for combining the references, such combination does not produce APPELLANTS disclosed and claimed invention. Neither Lin et al., Yu et al., nor Filipiak et al. disclose or suggest forming an ARC layer over sidewalls of a via opening without filling the via opening to reduce light reflection in a subsequent overlying trench patterning process. In addition, neither Filipiak et al., nor any combination with Yu et al. or Lin et al. disclose or suggest forming a first ARC layer overlying an IMD (insulating) layer **prior to** forming a via opening and conformally depositing a second ARC layer to cover via opening sidewalls **following**

formation of a via and prior to patterning an overlying trench as disclosed and claimed by APPELLANTS.

Examiner argues that "it would also have been obvious to apply at least one thin conformal ARC layer to the sidewalls of the holes or openings without filling the holes or openings before patterning an overlying resist layer to avoid reflective notching of the photoresist, as taught by Lin and disclosed by Filipiak".

APPELLANTS argue that Examiner is clearly mistaken that Lin et al. teach such a process or that Filipiak discloses such a process. Neither Lin et al. nor Filipiak et al. disclose, hint, or suggest forming an ARC layer over sidewalls of a via opening without filling the via opening prior to a trench patterning process to reduce light reflection from via sidewalls in the trench patterning process, a problem recognized and solved by APPELLANTS disclosed and claimed invention.

In summary, Lin et al. teach **filling the via opening** with a **protective material** to protect the via bottom portion in a subsequent trench etching process. Yu et al. teach using a

Ti/TiN etching hardmask which also functions as an ARC layer **for etching the via opening**. Filipiak et al. teach forming a multiple graded ARC layers over an insulating layer **prior to etching** via openings (see col 5, lines 14-40) and **do not disclose a dual damascene process**. The above teachings individually, or in combination, **do not** make out a *prima facie* case of obviousness nor recognize or solve the problem APPELLANTS have recognized and solved by their disclosed and claimed invention.

APPELLANTS disclosed and claimed invention recognizes and solves the problem of light reflections from via sidewalls to undercut a resist layer in a trench patterning process, without having to fill the via with a protective material and engage in a separate etchback process as in the method of Lin et al.

"We do not pick and choose among the individual elements of assorted prior art references to recreate the claimed invention, but rather we look for some teaching or suggestion in the references to support their use in a particular claimed combination" *Symbol Technologies, Inc. v. Opticon, Inc., 935 F.2d 1569, 19 USPQ2d 1241 (Fed. Cir. 1991).*

CLOSING

In summary, the Appellants have shown that their claimed invention is has not been shown to be *prima facie* obviousness by Examiner. Moreover, the cited references affirmatively show that APPELLANTS claimed invention is non-obvious. Since the prior art of record fails to disclose, teach or suggest APPELLANTS claimed invention, in addition to failing to recognize or solve the problem APPELLANTS have recognized and solved, the prior art of record supports the conclusion of non-obviousness. It is therefore respectfully submitted that Examiners final rejection of Appellants claims is improper under the statutory standard of 35 USC § 103(a) as interpreted by both the Board and the Courts.

The reversal of the final rejection is respectfully solicited from the Board.

Respectfully submitted,

Tung & Associates

By: _____

Randy W. Tung
Registration No. 31,311
Telephone: (248) 540-4040

CLAIM APPENDIX

1. A method for reducing light reflectance from via sidewalls in a photolithographic trench patterning dual damascene process comprising the steps of:

providing an inter-metal dielectric (IMD) layer comprising at least one via opening extending through a thickness thereof;

forming an antireflectance coating (ARC) layer over the IMD layer such that the ARC layer is formed over sidewalls of the at least one via opening without filling the at least one via opening; and,

depositing a photoresist layer over the IMD layer and photolithographically patterning a trench opening over the at least one via opening.

2. The method according to claim 1, wherein an etching stop layer is provided over said IMD layer.

3. The method of claim 2, wherein the etching stop layer is selected from the group consisting of silicon oxynitride and silicon nitride.

4. cancelled

5. cancelled

6. cancelled

7. The method of claim 1, wherein the ARC layer is selected from the group consisting of silicon oxynitride and titanium nitride.

8. The method of claim 1, wherein the ARC layer is formed within a range of thickness from about 100 Angstroms to about 1000 Angstroms.

9. cancelled

10. The method of claim 1, wherein the at least one via opening includes at least two via openings formed substantially adjacent to one another.

11. A method of reducing photoresist undercutting due to via sidewall light reflections in a dual damascene trench patterning process comprising the steps of:

providing an inter-metal dielectric (IMD) layer comprising a first anti-reflectance coating (ARC) layer over the IMD layer;

forming a via opening extending through a thickness portion of the IMD layer;

substantially conformally depositing a second ARC layer over said IMD layer and the via openings to cover the via opening sidewalls without filling the via opening; and,

forming a photoresist layer over the IMD layer and photolithographically patterning trench openings disposed at least partially over the via opening; and,

forming a photoresist layer over the IMD layer and photolithographically patterning trench openings disposed at least partially over the via opening.

12. cancelled

13. The method of claim 11, wherein an etching stop layer is provided over the IMD layer underlying the first ARC layer.

14. The method of claim 13, wherein the etching stop layer is selected from the group consisting of silicon oxynitride and silicon nitride.

15. The method of claim 11, wherein the first and second ARC layers are selected from the group consisting of silicon oxynitride and titanium nitride.

16. cancelled

17. The method of claim 11, wherein the second ARC layer is formed within a range of thickness from about 100 Angstroms to about 1000 Angstroms.

18. The method of claim 11, further comprising a second via opening formed substantially adjacent to the via opening.

19. The method of claim 11, further comprising repeating said method as part of a manufacturing process to form a multi-level interconnected semiconductor structure.

20. An improved method of reducing light reflectance from via sidewalls in a dual damascene trench patterning process comprising the steps of:

forming a first dielectric layer over an underlying substrate;

forming at least one second dielectric layer over said first dielectric layer;

forming at least one anti-reflectance coating (ARC) layer over the at least one dielectric layer;

forming at least one via opening through a thickness of the ARC layer, the at least one second dielectric layer, and the first dielectric layer;

forming at least one additional ARC layer substantially conformally over the at least one ARC layer and the at least one via opening to cover the at least one via opening without filling the at least one via opening;

forming a layer of photoresist over the at least one additional ARC layer; and,

photolithographically patterning a trench opening over the at least one via opening.

21. The method of claim 1, wherein the ARC layer is deposited according to a plasma enhanced chemical vapor deposition (PECVD) process.

22. The method of claim 11, wherein at least the second ARC layer is deposited according to a plasma enhanced chemical vapor deposition (PECVD) process.

23. The method of claim 1, wherein the ARC layer consists essentially of silicon oxynitride.

24. The method of claim 11, wherein the first and second ARC layers consist essentially of silicon oxynitride.

25. cancelled

26. cancelled

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Serial No.: 09/941,537 Examiner: J. S. Ruggles

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(5) SUMMARY OF THE INVENTION

The invention discloses a method for reducing light reflectance from via sidewalls in a photolithographic trench patterning dual damascene process to reduce undercutting of a photoresist layer thereby maintaining design distance between metal lines. (See Field of Invention Specification, paragraph

001; claim 1; Figures 2, items 25 and 26 and Figure 3, items 35 and 36). The method involves the steps of providing an inter-metal dielectric (IMD) layer comprising at least one via opening extending through a thickness thereof; forming an antireflectance coating (ARC) layer over the IMD layer such that the ARC layer is formed over sidewalls of the at least one via opening without filling the at least one via opening; and, depositing a photoresist layer over the IMD layer and photolithographically patterning a trench opening over the at least one via opening.

(6) ISSUES

1. Is the rejection of claim 15, under 35 USC second 112, second paragraph proper?

2. Is the rejection of claims 1-3, 7-8, 10-11, 13-15, and 17-24 under 35 USC § 103(a) as being unpatentable over Lin et al. (US 6,042,999) in view of Yu et al. (US 6,027,861) and further in view of Filipiak et al. (US 5,918,147) proper when such references does not teach or suggest the specifically claimed limitations in the present application?

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Claims 1-3, 7-8, 10-11, 13-15, 17-24 stand rejected under 35 USC 103(a) as being unpatentable over Lin et al., in view of Yu et al. (US Pat.No. 6,027,861) and further in view of Filipiak et al. (US Pat. No. 5,918,147).

a) Lin et al. teach a dual damascene process **by filling a via opening** with **protective material** prior to patterning an overlying trench in a dual damascene process (see Abstract). The protective material serves to protect the exposed material at the bottom of the via opening during a subsequent overlying trench etching process (see e.g., col 6, lines 10-14). Lin et al. teach first forming a via opening portion (see e.g., col 4, lines 55-67, col 5, lines 20-25). After removing the via pattern resist layer, Lin et al. teach depositing a protective material disclosed to be a BARC layer e.g., silicon oxynitride or an organic material **to fill the via opening**, (see e.g., col 5, lines 35-57, Figure 2C). Lin et al. then teach removing a portion of the protective material **from the filled via opening** to about a level of an intervening etch stop layer following patterning of the overlying trench. The protective material is first etched back followed by etching of the overlying trench or

simultaneously etched back with the trench etching (see col 5, lines 57-65 and col 5, lines 1-14).

Examiner argues "while not specifying an alternative embodiment requiring non-filling of the ARC layer in the holes or openings, it is readily apparent that adequate protection could also be obtained by using one or more ARC layers of sufficient thickness without necessarily requiring that the ARC material fill one or more via openings or holes.." . Examiner is impermissibly re-creating APPELLANTS disclosed invention by hindsight reasoning and can point to no suggestion, hint, or desirability in Lin et al. for doing what APPELLANTS have accomplished by their claimed invention.

The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." *In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).*

Examiner argues that the prior art disclosed in Lin et al. as shown in Figures 1C through 1F support Examiners argument since "these etch stop materials are also expected to inherently

function as ARC layers". Examiner provides no support for this statement of inherency. Lin et al. only disclose the use of SiN as an etch stop layer. Nevertheless, the fact that SiON is well known as having antireflectance properties is irrelevant to the issue of whether APPELLANTS claimed invention has been suggested or disclosed in Lin et al.

The prior art as disclosed in Lin et al. is referring to a totally different process of manufacturing dual damascenes. The prior art e.g., at col 2, lines 34-52) discloses depositing a **selective etch barrier layer** where SiN or SiON are disclosed to be useful materials with an appropriate etching selectivity. The etch barrier is deposited into **a trench opening** followed by etching **an opening through the etch barrier** at the bottom of the trench opening **followed by etching the via hole**. The etch barrier disclosed in the prior art by Lin et al. is not suggested or disclosed to have or require an anti-reflective property. However, even assuming arguendo, that such a suggestion was present in Lin et al., the teachings of Lin et al. do not produce APPELLANTS disclosed and claimed invention nor recognize or solve the problem that APPELLANTS have recognized and solved in their claimed invention:

"A method for reducing light reflectance from via sidewalls in a photolithographic trench patterning dual damascene process comprising the steps of:

forming an antireflectance coating (ARC) layer over the IMD layer such that the ARC layer is formed over sidewalls of the at least one via opening **without filling the at least one via opening**; and,

depositing a photoresist layer over the IMD layer and photolithographically patterning a trench opening over the at least one via opening."

Moreover, the prior art disclosed in Lin et al. that the Examiner relies on, would not work in the method of APPELLANTS since the purpose of the ARC layer is to reduce reflections in an overlying trench line patterning process **following formation of a via opening**. Indeed, Lin et al. affirmatively teach away from APPELLANTS claimed invention by requiring either a separate or simultaneous etching step to remove a portion of the protective material during etching an overlying trench (col 5, line 62 - col 6, line 14). The principal of operation of Lin et al. is completely different than the principal of operation of the method of Lin et al.

"Obviousness can only be established by combining or modifying the

teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art." *In re Fine, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988); In re Jones, 958 F.2d 347, 1 USPQ2d 1941 (Fed. Cir. 1992).*

"If the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims prima facie obvious." *In re Ratti, 270 F.2d 810, 123, USPQ 349 (CCPA 1959).*

"To establish inherency, the extrinsic evidence must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill." *In re Oelrich, 666 F.2d 578, 581-582, 212 USPQ 323, 326 (CCPA 1981).*

Lin et al., further do not teach, suggest or disclose forming a first ARC layer over the IMD layer **prior** to forming via openings followed by **forming** a second ARC layer to cover via opening sidewalls **without filling the at least one via opening** as claimed by APPELLANTS in amended claim 11. Neither do Lin et al. disclose the problem of photoresist undercutting from via sidewall reflections or disclose APPELLANTS claimed limitations in claims 10, and 18.

Lin et al. further do not teach forming a first ARC layer prior to forming the via opening and a second ARC layer to cover via opening sidewalls following formation of a via opening as claimed by APPELLANTS in independent claim 11 and 20 and independent claim 20, or including an etch stop layer over the IMD layer as claimed in claims 2, 13, and 20 (second dielectric layer). Examiner has not made out a *prima facie* case of obviousness according to Lin et al. with respect to above limitations.

b) Yu et al. teach a method for etching sub-quarter micron openings in dielectric insulating layers by using a thin layer DUV photoresist (see Abstract). In one embodiment, Yu et al. disclose forming a via opening for filling with a tungsten plug by using a Ti/TiN etching hardmask which also functions as an ARC layer for etching the via opening (col 4, lines 58-62). The via is then etched with the Ti/TiN layer hard mask providing high selectivity for etching the insulating layer (col 6, lines 19-24).

Yu et al. does not suggest disclose or suggest depositing an ARC layer to fill the via opening as taught by Lin et al., nor disclose or suggest forming an ARC layer formed over sidewalls of

a via opening without filling the via opening prior to patterning an overlying trench portion in a dual damascene process as claimed by APPELLANTS.

There is no apparent reason for combining the teachings of Yu et al. with Lin et al. However, even assuming *arguendo* proper combination of Yu et al. and Lin et al., such combination does not produce APPELLANTS claimed invention. The disclosure of Yu et al. in forming a Ti/TiN hardmask layer that also functions as an ARC layer does not help Examiner in making out a *prima facie* case of obviousness. APPELLANTS do not disclose or claim a Ti/TiN layer but rather disclose a TiN ARC layer as one element of a Markush group for forming a first or second ARC layer. Yu et al. do not discuss, disclose or suggest the desirability of depositing an ARC layer to cover the via opening sidewalls without filling the via opening prior to a trench patterning process overlying the via. The teachings of Yu et al. do not recognize or solve the problems APPELLANTS have recognized and solved by their claimed invention. Yu et al. does not help Examiner in establishing a *prima facie* case of obviousness.

c) Filipiak et al. generally discloses types of ARC layers such as silicon oxynitride and titanium nitride in the background of

the invention (see col 1, lines 10-20) as well as teaching the use of multiple ARC layers including forming inorganic ARC layers, e.g., silicon oxynitride with a continuously graded composition or including a plurality of discrete portions that make up the antireflective layer (see col 2, lines 17-27, col 3, lines 21-30). There is no apparent motivation for combining Filipiak et al. with either Yu et al. or Lin et al. For example, Filipiak et al. disclose the use ARC layers **prior to** etching via openings, and further, do not disclose a dual damascene process.

Nevertheless, assuming *arguendo*, a proper motivation for combining the references, such combination does not produce APPELLANTS disclosed and claimed invention. Neither Lin et al., Yu et al., nor Filipiak et al. disclose or suggest forming an ARC layer over sidewalls of a via opening without filling the via opening to reduce light reflection in a subsequent overlying trench patterning process. In addition, neither Filipiak et al., nor any combination with Yu et al. or Lin et al. disclose or suggest forming a first ARC layer overlying an IMD (insulating) layer **prior to** forming a via opening and conformally depositing a second ARC layer to cover via opening sidewalls **following**

formation of a via and prior to patterning an overlying trench as disclosed and claimed by APPELLANTS.

Examiner argues that "it would also have been obvious to apply at least one thin conformal ARC layer to the sidewalls of the holes or openings without filling the holes or openings before patterning an overlying resist layer to avoid reflective notching of the photoresist, as taught by Lin and disclosed by Filipiak".

APPELLANTS argue that Examiner is clearly mistaken that Lin et al. teach such a process or that Filipiak discloses such a process. Neither Lin et al. nor Filipiak et al. disclose, hint, or suggest forming an ARC layer over sidewalls of a via opening without filling the via opening prior to a trench patterning process to reduce light reflection from via sidewalls in the trench patterning process, a problem recognized and solved by APPELLANTS disclosed and claimed invention.

In summary, Lin et al. teach **filling the via opening** with a **protective material** to protect the via bottom portion in a subsequent trench etching process. Yu et al. teach using a

Ti/TiN etching hardmask which also functions as an ARC layer **for etching the via opening**. Filipiak et al. teach forming a multiple graded ARC layers over an insulating layer **prior to etching** via openings (see col 5, lines 14-40) and **do not disclose a dual damascene process**. The above teachings individually, or in combination, **do not** make out a *prima facie* case of obviousness nor recognize or solve the problem APPELLANTS have recognized and solved by their disclosed and claimed invention.

APPELLANTS disclosed and claimed invention recognizes and solves the problem of light reflections from via sidewalls to undercut a resist layer in a trench patterning process, without having to fill the via with a protective material and engage in a separate etchback process as in the method of Lin et al.

"We do not pick and choose among the individual elements of assorted prior art references to recreate the claimed invention, but rather we look for some teaching or suggestion in the references to support their use in a particular claimed combination" *Symbol Technologies, Inc. v. Opticon, Inc., 935 F.2d 1569, 19 USPQ2d 1241 (Fed. Cir. 1991).*

CLOSING

In summary, the Appellants have shown that their claimed invention is has not been shown to be *prima facie* obviousness by Examiner. Moreover, the cited references affirmatively show that APPELLANTS claimed invention is non-obvious. Since the prior art of record fails to disclose, teach or suggest APPELLANTS claimed invention, in addition to failing to recognize or solve the problem APPELLANTS have recognized and solved, the prior art of record supports the conclusion of non-obviousness. It is therefore respectfully submitted that Examiners final rejection of Appellants claims is improper under the statutory standard of 35 USC § 103(a) as interpreted by both the Board and the Courts.

The reversal of the final rejection is respectfully solicited from the Board.

Respectfully submitted,

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CLAIM APPENDIX

1. A method for reducing light reflectance from via sidewalls in a photolithographic trench patterning dual damascene process comprising the steps of:

providing an inter-metal dielectric (IMD) layer comprising at least one via opening extending through a thickness thereof;

forming an antireflectance coating (ARC) layer over the IMD layer such that the ARC layer is formed over sidewalls of the at least one via opening without filling the at least one via opening; and,

depositing a photoresist layer over the IMD layer and photolithographically patterning a trench opening over the at least one via opening.

2. The method according to claim 1, wherein an etching stop layer is provided over said IMD layer.

3. The method of claim 2, wherein the etching stop layer is selected from the group consisting of silicon oxynitride and silicon nitride.

4. cancelled

5. cancelled

6. cancelled

7. The method of claim 1, wherein the ARC layer is selected from the group consisting of silicon oxynitride and titanium nitride.

8. The method of claim 1, wherein the ARC layer is formed within a range of thickness from about 100 Angstroms to about 1000 Angstroms.

9. cancelled

10. The method of claim 1, wherein the at least one via opening includes at least two via openings formed substantially adjacent to one another.

11. A method of reducing photoresist undercutting due to via sidewall light reflections in a dual damascene trench patterning process comprising the steps of:

providing an inter-metal dielectric (IMD) layer comprising a first anti-reflectance coating (ARC) layer over the IMD layer;

forming a via opening extending through a thickness portion of the IMD layer;

substantially conformally depositing a second ARC layer over said IMD layer and the via openings to cover the via opening sidewalls without filling the via opening; and,

forming a photoresist layer over the IMD layer and photolithographically patterning trench openings disposed at least partially over the via opening; and,

forming a photoresist layer over the IMD layer and photolithographically patterning trench openings disposed at least partially over the via opening.

12. cancelled

13. The method of claim 11, wherein an etching stop layer is provided over the IMD layer underlying the first ARC layer.

14. The method of claim 13, wherein the etching stop layer is selected from the group consisting of silicon oxynitride and silicon nitride.

15. The method of claim 11, wherein the first and second ARC layers are selected from the group consisting of silicon oxynitride and titanium nitride.

16. cancelled

17. The method of claim 11, wherein the second ARC layer is formed within a range of thickness from about 100 Angstroms to about 1000 Angstroms.

18. The method of claim 11, further comprising a second via opening formed substantially adjacent to the via opening.

19. The method of claim 11, further comprising repeating said method as part of a manufacturing process to form a multi-level interconnected semiconductor structure.

20. An improved method of reducing light reflectance from via sidewalls in a dual damascene trench patterning process comprising the steps of:

forming a first dielectric layer over an underlying substrate;

forming at least one second dielectric layer over said first dielectric layer;

forming at least one anti-reflectance coating (ARC) layer over the at least one dielectric layer;

forming at least one via opening through a thickness of the ARC layer, the at least one second dielectric layer, and the first dielectric layer;

forming at least one additional ARC layer substantially conformally over the at least one ARC layer and the at least one via opening to cover the at least one via opening without filling the at least one via opening;

forming a layer of photoresist over the at least one additional ARC layer; and,

photolithographically patterning a trench opening over the at least one via opening.

21. The method of claim 1, wherein the ARC layer is deposited according to a plasma enhanced chemical vapor deposition (PECVD) process.

22. The method of claim 11, wherein at least the second ARC layer is deposited according to a plasma enhanced chemical vapor deposition (PECVD) process.

23. The method of claim 1, wherein the ARC layer consists essentially of silicon oxynitride.

24. The method of claim 11, wherein the first and second ARC layers consist essentially of silicon oxynitride.

25. cancelled

26. cancelled